Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously presented) A pipeline synchronization device for transferring data between clocked devices having different clock frequencies, comprising:

a mousetrap buffer for exchanging data with one of the clocked devices, the mousetrap buffer including a signalling output for coordinating the data exchange with the clocked device, and

a synchronizer that is configured to synchronize a change in the signalling output with a clock of the clocked device.

2. (Previously presented) The device of claim 1, wherein the synchronizer is configured to synchronize the change in the signalling output with a high phase or a low phase of the clock of the external device.

3. (Previously presented) The device of claim 2, wherein the synchronizer is configured to delay a transfer of the change in the signalling output until the clock of the clocked device is in a given state.

4. (Previously presented) The device of claim 3, wherein the synchronizer includes a synchronizing latch that includes: a synchronizing input for receiving the signalling output, a synchronizing output for outputting the received signalling output to the clocked device and a control input for enabling the output of the received signalling output to the clocked device.

5. (Previously presented) The device of claim 4, wherein the synchronizer includes an EXNOR-gate having two inputs and one output, the inputs of the EXNOR-gate being connected to the synchronizing input and output of the synchronizing latch, and the synchronizer includes a wait-component having an input connected to the output of the EXNOR-gate, an input connected to the clock of the clocked device and an output connected to the control input of the synchronizing latch.

6. (Previously presented) The device of claim 5, wherein the wait-component is configured to signal a change from low to high of the input if the clock of the clocked device is in a given state, and to signal a change from high to low of the input irrespective of the state of the clock of the clocked device.

7. (Previously presented) The device of claim 6, wherein the wait-component comprises an inverter and an arbiter having an input for receiving an inverted clock signal from the inverter, and an input for receiving the output of the EXNOR-gate and an output for transmitting the input.

8. (Previously presented) The device of claim 1, wherein the synchronizer is configured to synchronize the change in the signalling output with a rising and/or a falling edge of the clock of the clocked device.

9. (Previously presented) The device of claim 8, wherein the synchronizer includes two synchronizers that are configured to delay a transfer of a change in the signalling output until the clock of the clocked device is in a given state, wherein a first of the two synchronizers is configured to transfer a change in the signalling output of a first mousetrap buffer to the clocked device and wherein a second of the two synchronizers receives an inverted clock of the clocked device and is configured to transfer a signalling output of a second mousetrap buffer to the first mousetrap buffer.

10. (Previously presented) The device of claim 8, wherein the synchronizer includes an edge synchronizer that includes two wait-components, each being configured to signal a change from low to high in the input if a received clock is in a given state, and to signal a change from high to low in the input irrespective of the state of the received clock, wherein a first of the two wait-components is configured to receive the clock of the clocked device and to signal a change in its input to the clocked device, and wherein a second of the two wait components is configured to receive an inverted clock from the clocked device and to signal a change in its input to the first wait component.

11. (Previously presented) The device of claim 10, wherein the synchronizer includes a synchronizing latch having a synchronizing input for receiving the signalling output, a synchronizing output for outputting the received signalling output to the clocked device and a control input for enabling the output of the received signalling output to the clocked device.

12. (Previously presented) The device of claim 11, wherein the synchronizer includes an EXNOR-gate having two inputs and one output, the inputs of the EXNOR-gate being connected to the synchronizing input and output of the synchronizing latch, and the synchronizer includes an edge synchronizer having an input connected to the output of the EXNOR-gate, an input connected to the clock of the clocked device and an output connected to the control input of the synchronizing latch.

13. (Previously presented) The device of claim 1, wherein the mousetrap buffer is configured to receive data from the clocked device and the mousetrap buffer includes a signalling output for acknowledging the receipt of data to the clocked device.

14. (Previously presented) The device of claim 1, wherein the mousetrap buffer is configured to transfer data to the clocked device and the mousetrap buffer includes a signalling output for requesting the transfer of data to the clocked device.

15. (Previously presented) The device of claim 13, wherein the mousetrap buffer includes an EXOR-gate for receiving a read request signal and a read acknowledge signal, a latch having a control input for enabling and disabling the receiving and transferring of data, wherein the synchronizer is configured to synchronize an output of the EXOR-gate with the clock of the clocked device and to supply the output of the EXOR-gate to the control input of the latch.

16. (Previously presented) The device of claim 15, wherein the synchronizer is configured to synchronize a change in the output of the EXOR-gate with a rising and/or a falling edge of the clock of the clocked device.

17. (Previously presented) A method for transferring data between clocked devices having different clock frequencies, comprising:

exchanging data with one of the clocked devices via a mousetrap buffer that is configured to output a signal for coordinating the data exchange with the clocked device, and

synchronizing changes in the output signal with the clock of the clocked device.